# Laboratory Report # 4

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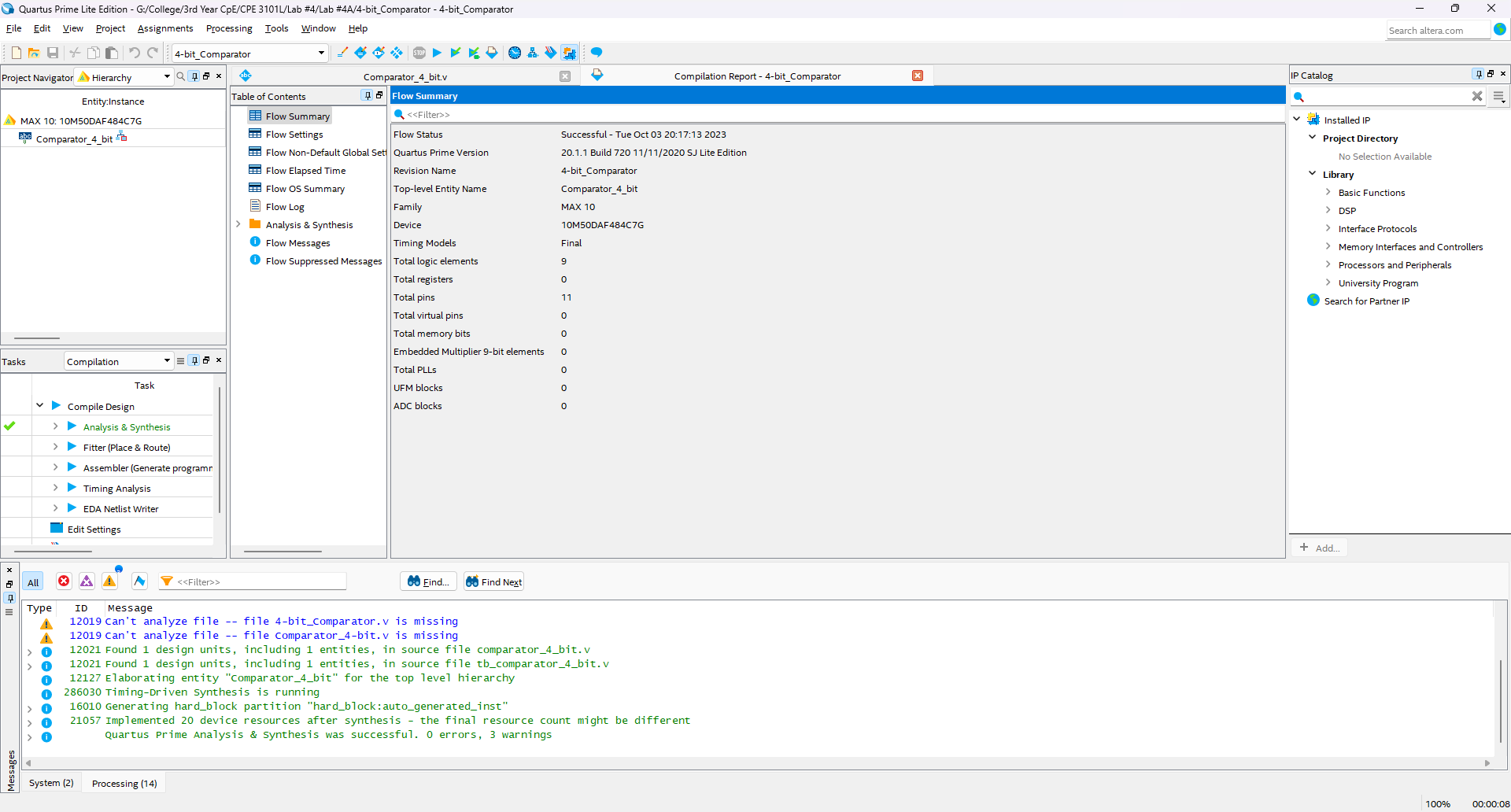
**Laboratory Exercise Title:** Dataflow Modeling of Combinational Circuits

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

**Exercise 3A:**



**Figure 1: Proof of Successful Design Synthesis of 4-bit Comparator**

**A computer screen shot of a black screen

Description automatically generated**

A[3] A[2] A[1] A[0]

1 1 0 1

B[3] B[2] B[1] B[0]

1 0 1 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 1 1

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

0 0 1 1

B[3] B[2] B[1] B[0]

0 0 1 1

R[2] R[1] R[0]

0 1 0

A[3] A[2] A[1] A[0]

0 0 0 0

B[3] B[2] B[1] B[0]

1 1 1 1

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

0 1 0 1

B[3] B[2] B[1] B[0]

0 1 0 1

R[2] R[1] R[0]

0 1 0

A[3] A[2] A[1] A[0]

1 1 1 1

B[3] B[2] B[1] B[0]

0 0 0 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

1 0 1 0

B[3] B[2] B[1] B[0]

1 1 0 0

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

0 1 0 1

B[3] B[2] B[1] B[0]

0 0 1 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

0 0 1 0

B[3] B[2] B[1] B[0]

0 1 0 1

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

1 1 0 0

B[3] B[2] B[1] B[0]

1 1 0 0

R[2] R[1] R[0]

0 1 0

**Figure 2: Proof of Successful Simulation Results of 4-bit Comparator**