# Laboratory Report # 4

**Name:** Machacon, Zach Riane  **Date Completed:** September 30, 2023

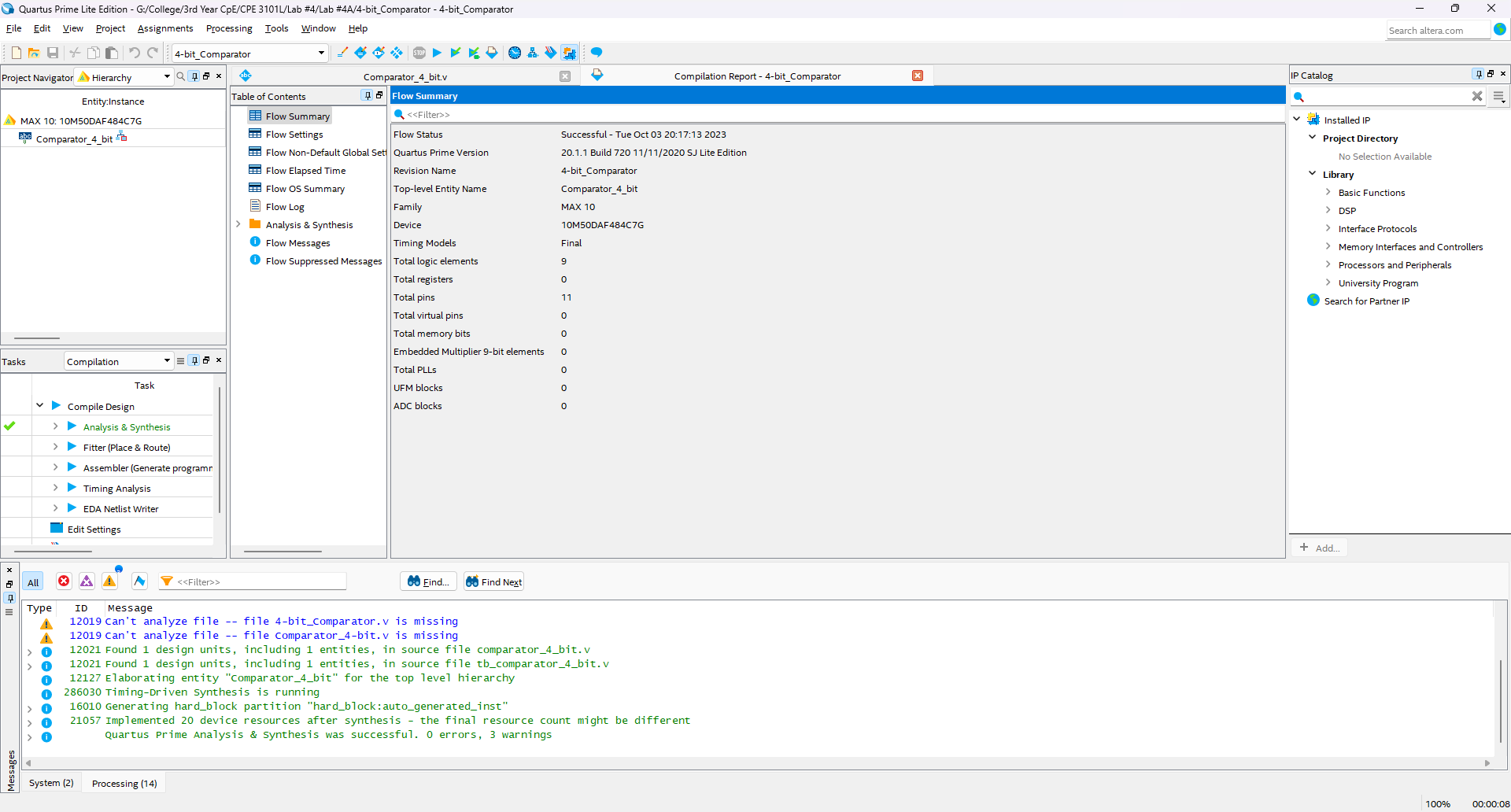
**Laboratory Exercise Title:** Dataflow Modeling of Combinational Circuits

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

**Exercise 3A:**



**Figure 1: Proof of Successful Design Synthesis of 4-bit Comparator**

**A computer screen shot of a black screen

Description automatically generated**

A[3] A[2] A[1] A[0]

1 1 0 1

B[3] B[2] B[1] B[0]

1 0 1 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 1 1

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

0 0 1 1

B[3] B[2] B[1] B[0]

0 0 1 1

R[2] R[1] R[0]

0 1 0

A[3] A[2] A[1] A[0]

0 0 0 0

B[3] B[2] B[1] B[0]

1 1 1 1

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

0 1 0 1

B[3] B[2] B[1] B[0]

0 1 0 1

R[2] R[1] R[0]

0 1 0

A[3] A[2] A[1] A[0]

1 1 1 1

B[3] B[2] B[1] B[0]

0 0 0 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

1 0 1 0

B[3] B[2] B[1] B[0]

1 1 0 0

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

0 1 0 1

B[3] B[2] B[1] B[0]

0 0 1 0

R[2] R[1] R[0]

1 0 0

A[3] A[2] A[1] A[0]

0 0 1 0

B[3] B[2] B[1] B[0]

0 1 0 1

R[2] R[1] R[0]

0 0 1

A[3] A[2] A[1] A[0]

1 1 0 0

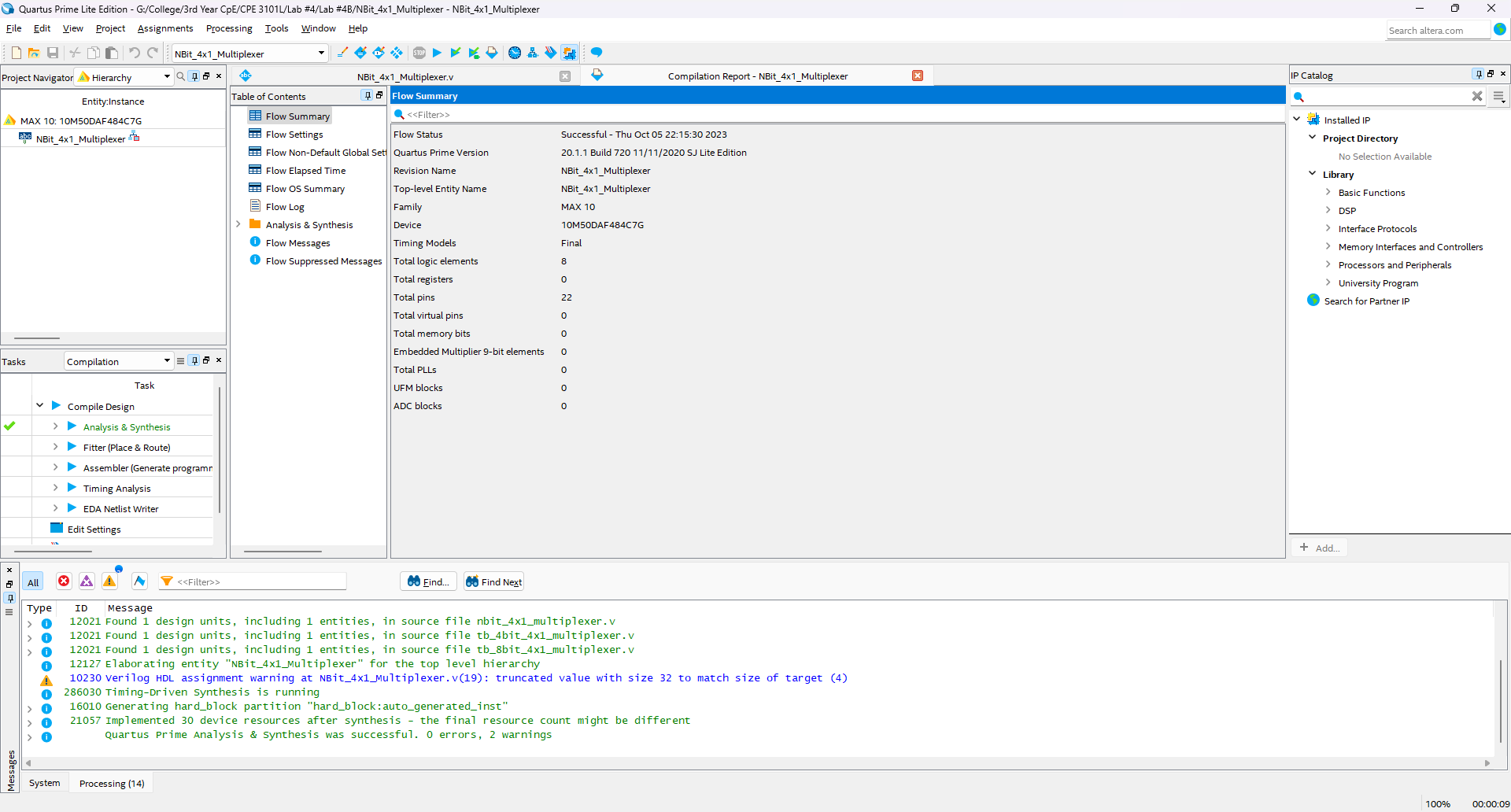
B[3] B[2] B[1] B[0]

1 1 0 0

R[2] R[1] R[0]

0 1 0

**Figure 2: Proof of Successful Simulation Results of 4-bit Comparator**



**Figure 3: Proof of Successful Design Synthesis of n-Bit 4-to-1 Line Multiplexer**

**A screenshot of a computer

Description automatically generated**

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 0 0

C[3] C[2] C[1] C[0]

0 0 1 0

D[3] D[2] D[1] D[0]

0 0 0 1

Y[3] Y[2] Y[1] Y[0]

0 0 0 1

S[1] S[0]

1 1

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 0 0

C[3] C[2] C[1] C[0]

0 0 1 0

D[3] D[2] D[1] D[0]

0 0 0 1

Y[3] Y[2] Y[1] Y[0]

0 0 1 0

S[1] S[0]

1 0

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 0 0

C[3] C[2] C[1] C[0]

0 0 1 0

D[3] D[2] D[1] D[0]

0 0 0 1

Y[3] Y[2] Y[1] Y[0]

0 1 0 0

S[1] S[0]

0 1

A[3] A[2] A[1] A[0]

1 0 0 0

B[3] B[2] B[1] B[0]

0 1 0 0

C[3] C[2] C[1] C[0]

0 0 1 0

D[3] D[2] D[1] D[0]

0 0 0 1

Y[3] Y[2] Y[1] Y[0]

1 0 0 0

S[1] S[0]

0 0

**Figure 3: Proof of Successful Simulation Results of 4-Bit 4-to-1 Line Multiplexer**

**A screen shot of a computer

Description automatically generated**

S = 11

A = 01010101

B = 10101010

C = 11110000

D = 00001111

Y = 00001111

S = 10

A = 01010101

B = 10101010

C = 11110000

D = 00001111

Y = 11110000

S = 00

A = 01010101

B = 10101010

C = 11110000

D = 00001111

Y = 01010101

S = 01

A = 01010101

B = 10101010

C = 11110000

D = 00001111

Y = 10101010

**Figure 4: Proof of Successful Simulation Results of 8-Bit 4-to-1 Line Multiplexer**